**Lab Assignment 3**

**Task 1 – watch the video**

Introduction to Verilog

<https://www.youtube.com/watch?v=0age83XI8Z4>

Do the following:

1. Simplify the Boolean function
2. Write a truth table for each problem
3. Draw a schematic diagram for (problem 1,2) then test using wave form then compare with truth table whether your circuit produced same output or not?
4. Write a Verilog code for (problem 3,4) then test using wave form then compare with truth table whether your circuit produced same output or not?

Problems:

1. F(A, B, C)=ABC + A’BC + AB’C + ABC
2. F(A, B, C, D)=ABCD’ + A’BC D+ AB’CD’ + ABC
3. F(A, B, C, D)= m{1,3,5,7,9,11,13}
4. F(A, B, C, D)=m {1,2,4, 6, 7, 9, 10, 11, 13}